CHARACTERIZATION OF HIGH-DENSITY MICROMACHINED INTERCONNECTS

Jeremy L. Haley* and Rhonda Franklin Drayton

Department of Electrical and Computer Engineering, University of Minnesota,
200 Union Street St. S.E., Minneapolis, MN 55455, USA; drayton@ece.umn.edu

***Abstract* — Silicon micromachining is used to locally reduce the substrate height of large diameter wafers in order to maintain single-mode microstrip propagation. Effective dielectric constant and attenuation are shown up to 45 GHz for a 50-ohm microstrip line that is printed across a thick (400 μm) and thin (100μm) silicon area. Discontinuity effects for the dielectric and conductor show lower reflection (-10dB above 15 GHz) and smoother transmission characteristics for the abrupt conductor transition compared to the tapered one. Loss performance of the reduced height interconnects are comparable to full height constant thickness designs and interconnect densities as high a factor of 4 can be achieved.**

I. INTRODUCTION

In spite of beneficial system-level software strategies to improve high-speed system performance (e.g. coding and resource allocation algorithms) hardware implementations still present significant constraints on future advances in high-speed communications and computing applications. Electrical pathways between components, subsystems, and processing units are important for maintaining signal integrity. Hence, integration schemes that allow interconnected components to be in close proximity alleviate deleterious effects that arise in long signal paths from multiple interfaces.

High frequency integrated circuit applications can benefit tremendously from the large volume, low cost advantages of silicon fabrication processes. The larger diameter wafers, which improve cost per die, result in increased wafer thickness that can be detrimental to high speed interconnect performance due to the excitation of unwanted substrate modes. High-speed semiconductor-based design solutions are needed, therefore, that incorporate manufacturing trends with high frequency design requirements to optimize performance and cost.

One design solution is to selectively reduce the substrate areas that will accommodate high speed interconnects. This approach offers two primary benefits: (1) the capability to design a substrate thickness that will ensure fundamental-mode propagation and (2) the ability to increase input/output interconnect density for a given interconnect characteristic impedance. Such an approach can be accomplished using silicon (Si) micromachining, a technology that has resulted in improved Si-based high frequency circuit and package designs [1]-[2]. By selectively thinning regions of a full height wafer to achieve a desired thickness, optimum interconnect performance can be achieved while maintaining the overall mechanical strength of the remaining substrate.

In this study, constant impedance (50Ω) lines are printed across full height and reduced-height substrate regions. Various designs are considered based on different reduced height values and conductor transitions. Discontinuity effects on interconnect performance are evaluated and electrical parameters, such as attenuation and effective dielectric, are determined for various micromachined designs.

II. DESIGN/FABRICATION APPROACH

A. Design of reduced thickness microstrip lines

Microstrip designs based on 50Ω characteristic impedance (Z_0) are developed on full-thickness silicon and transitioned to a reduced height micromachined section as shown in Fig.1-Side view. In this approach, the propagation and loss effects (i.e. effective dielectric constant and characteristic impedance) are evaluated. Since the lines are printed on a modified dielectric section associated with a pyramidal cavity profile, the impact of the sloping sidewalls are investigated to determine the effect on interconnect performance between the full- and reduced-thickness sections. Two conductor transitions were considered: *abrupt* and *taper* (see Fig. 1-Top view). The conductor transition begins at the start of the etched cavity region and the taper one ends at the start of the reduced-thickness section.

These structures are electrically characterized by measuring two-port S-parameters of the microstrip lines using Cascade Microtech 150 micron pitch, on-wafer, air-

* Mr. Haley is now at the Department of Electrical and Computer Engineering of University of Illinois, Urbana, IL, 60801.

0-7803-6540-2/01/$10.00 (C) 2001 IEEE

coplanar probes and station. All device under test (DUT) designs include a coplanar waveguide-to-microstrip feed-

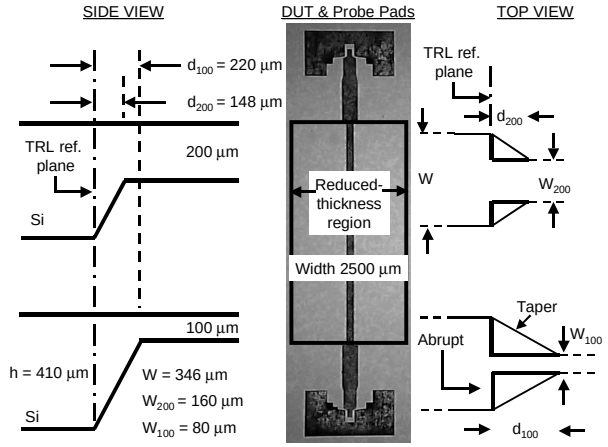

Fig. 1. Reduced thickness designs and microstrip photograph

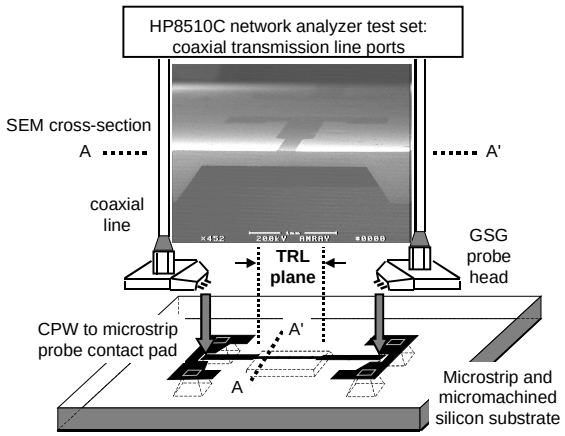

Fig. 2. Microstrip DUT, SEM image, and measurement setup.

line launch on each end (see Fig.2). The reference plane at the inputs to the micromachined DUT is established using microstrip calibration standards located on the same silicon substrate and is processed using the NIST algorithm, Multi-Cal: DEEMBED [3]. In each case the DUT is 10 mm long between corresponding TRL reference planes.

B. Fabrication of reduced thickness microstrip lines

The microstrip lines are developed using standard IC processes and are described in four phases shown in Fig.3. A 400 μm double-side polished, high resistivity silicon wafer (> 2000 ohm-cm with (100) orientation) is used. All conductors are printed on top of masking films consisting of 1000 Å LPCVD silicon nitride and 1.8 microns of thermal silicon dioxide deposited above the silicon surface.

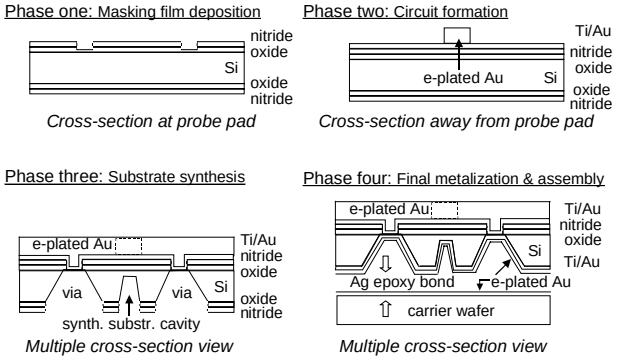

Fig. 3. Microfabrication process flow.

In phase one, dry (RIE) and wet (BOE) etches are used to remove the nitride and oxide films to form a direct contact between the upper ground electrode and the backside one. Four-micron thick gold microstrip lines are formed by electroplating a Ti/Au/Ti seed layer (400/1500/400 Å) as seen in the cross-section shown in Fig.3-Phase2. Next, the nitride and oxide films are removed from the bottom of the wafer, and the vias and cavities are etched using tetra-methyl ammonium hydroxide (TMAH), which anisotropically etches silicon to produce the pyramidal profile indicated in Fig.3-Phase3. After etching, the masking films are removed on the backside, and the lower non-planar surface is metalized with a Ti/Au (400/1000 Å) seed layer that is RF sputtered and electroplated to 4 microns. All wafers are attached to a carrier wafer using conducting epoxy.

The Scanning Electron Microscope (SEM) image in Fig.2 shows the cross-section of the microstrip line on reduced-thickness substrate with conductor transition and probe pad visible in the background.

III. Discussion and Results

A full-height microstrip is measured and simulated to establish a benchmark for reflection and insertion loss data (see Fig. 4). In Figs. 5-8, measured and simulated reflection and transmission response data is shown for 50-ohm lines having *abrupt* and *taper* conductor transitions illustrated in Fig.1 for various substrate heights. Design simulations have been generated using ADS [5] software to evaluate the accuracy of these fast CAD tools for predicting response of micromachined transitions. While full-wave solvers can be used to determine the most accurate response, long computational times make them more appropriate for analysis rather than design.

The micromachined line is modeled, where the appropriate transition element (step or taper) is used to represent the conductor discontinuity for the abrupt and

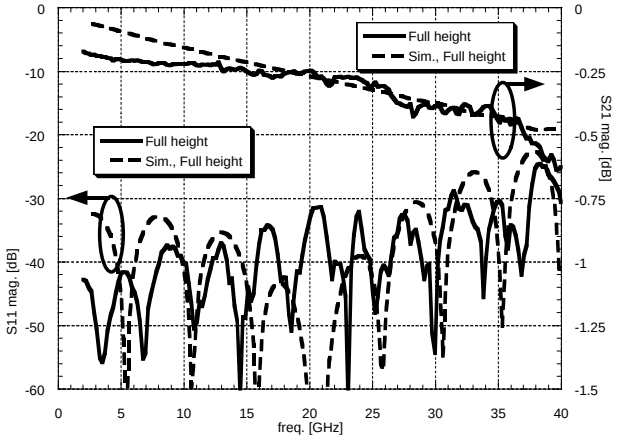

Fig. 4. Magnitudes of S_{11} and S_{21} for 50-ohm microstrip lines on regular substrates.

taper design, respectively. The substrate parameters are based on ε_R of 11.7, tanδ of 0.003, and gold conductor thickness of 4 μm. The transition element requires definition of the width (initial and final), length, and substrate parameters. See Fig.1 for the associated conductor transition dimensions.

At the micromachined junctions, the designation of the appropriate substrate height to the transition element is not intuitive. Simulation cases presented in Figs. 5-8 include labels indicating transition substrate designation in the model. Since the *abrupt* conductor step occurs at the onset of the etched substrate slope, these transition elements are assigned to the full height case. For the *taper* junction, the dielectric and strip width variations make substrate designation ambiguous. Both 100 and 200 micron thick *taper* cases were studied, however, only 100 micron data is presented since the more extreme change in substrate height (i.e. 400 to 100 microns) resulted in the largest impact on interconnect performance.

Reflection response data for the *abrupt* and *taper* cases are plotted in Figs. 5 and 7. The return loss increases as the substrate height decreases. Above 15 GHz, the return loss of the *taper* case shows a 10dB higher response compared to the *abrupt* design. For design purposes, ADS was used to predict an estimated response of the taper, where the transition element has been simulated with substrate references to full and reduced heights. Experimental data results were bounded by this prediction as shown in Fig. 7 and are being evaluated with more accurate full-wave solvers.

Transmission responses for the two conductor discontinuity designs are plotted in Figs. 6 and 8 and show increased insertion loss for reduced substrate heights. Since the lines are designed for 50Ω characteristic impedance, the increased attenuation for the narrow lines

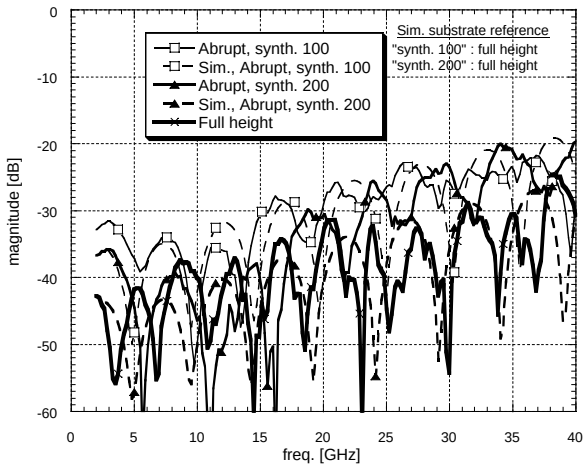

Fig. 5. Magnitude S_{11} for 50-ohm microstrip lines on regular and synthesized substrates with abrupt transition.

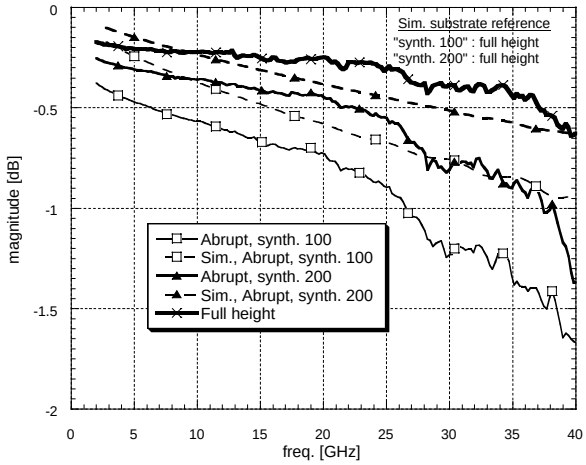

Fig. 6. Magnitude S_{21} for 50-ohm microstrip lines on regular and synthesized substrates with abrupt transition.

on thin substrates are due to higher conductor losses associated with current crowding. The onset of pronounced undulations in the simulated and measured *taper* transmission response above 20 GHz arises from pronounced reflections observed in Fig.7.

Relations between complex propagation constant and S-parameters for a lossy transmission line [4] are used to determine the effective dielectric constant (ε_{eff}) and attenuation constant (α). The ε_{eff} variation with frequency shown in Fig. 9 is for the *abrupt* case only. Since the reduced height substrate increases the proportion of fields in the air region, the concentration of fields above the substrate leads to a decrease in effective dielectric constant. The 100 micron reduced-thickness microstrip exhibits much less dispersion than the full height benchmark in spite of the increased loss performance.

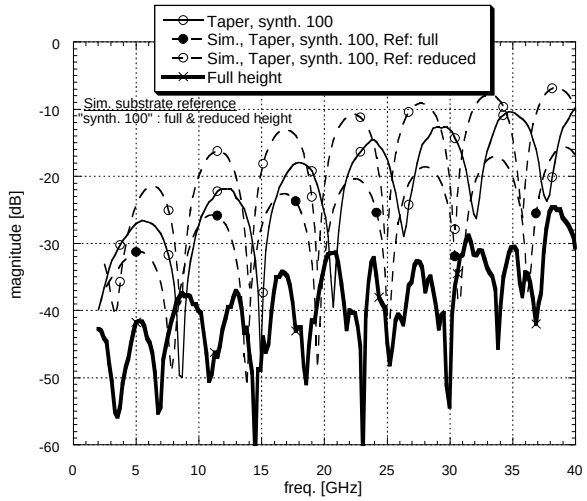

Fig. 7. Magnitude S_{11} for 50-ohm microstrip lines on regular and synthesized substrates with taper transition

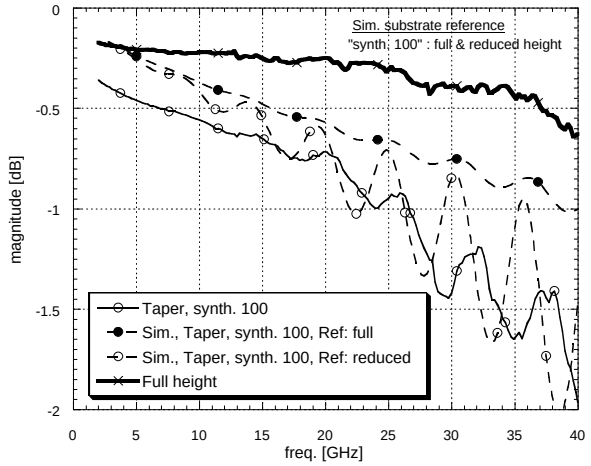

Fig. 8. Magnitude S_{21} for 50-ohm microstrip lines on regular and synthesized substrates with taper transition.

Hence, these types of interconnects are less susceptible to signal spreading. Additionally, the lines are physically small enough to provide much higher interconnect densities in circuits and integrated packages than designs based on full thickness substrates. The attenuation constant shown in Fig.9 verifies the expected trend of increased interconnect loss on thinner substrates. The measured data is also consistent with expected performance of designs on constant height wafers.

IV. Conclusion

Microstrip characteristics on the regular full-height benchmark and those of half- and quarter-height micro-machined substrates are evaluated. The *abrupt* conductor strip width configuration demonstrates wideband, low return losses compared to the *taper* that are lower by 10 dB above 15 GHz. Interconnects on thinner substrates show less dispersion compared to thicker designs. Finally, higher interconnect densities up to four-fold are possible, which is important and promising for high-speed computing and integrated packages.

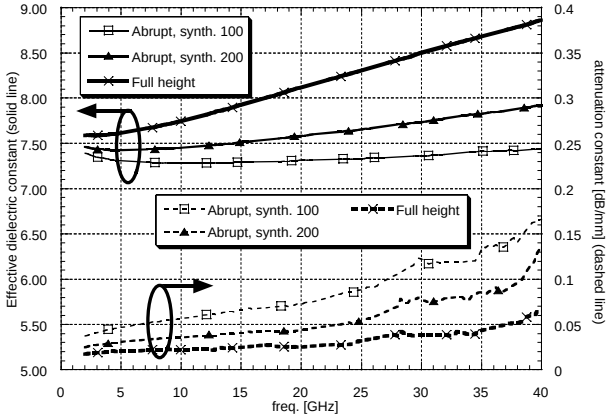

Fig. 9. Measured effective dielectric constant and attenuation constant for 50-ohm microstrip lines on regular and synthesized substrates.

Acknowledgement

This work has been supported by a grant from the National Science Foundation: ECS-9996017.

References

[1] R. F. Drayton, R. M. Henderson, and L. P. B. Katehi, "Monolithic packaging concepts for high isolation in circuits and antennas," *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-46, no. 7, pp. 900-906, July 1998.

[2] R. F. Drayton, S. Pacheco, J-G. Yook, and L. P. B. Katehi, "Micromachined filters on synthesized substrates," *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-49, no. 2, pp. 308-314, February 2001.

[3] R. B. Marks and D. F. Williams, Program MultiCal, rev. 1.00, NIST August 1995.

[4] W. R. Eisenstadt and Y. Eo, "S-parameter-based IC interconnect transmission line characterization," *IEEE Trans. Components, Hybrids & Manufacturing Tech.*, vol. 15, no. 4, pp. 483-490, August 1992.

[5] Advanced Design System, rev.1.3, Agilent Technologies, Palo Alto, CA, 1999.